An application of direct digital frequency synthesizer at frequency transform circuit

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Abstract: This paper introduces a solution of frequency converter that generates a 10.24MHz high-stability signal from a 10MHz high-stability reference source. This design is based on Direct Digital Synthesis (DDS). For DDS devices, internal or external high-order multiplier circuits are no longer used, and the output frequency and phase can be step-adjusted. The synthesized 10.24MHz signal can be used as a high-stability clock reference of the phase-locked loop circuit after subsequent noise suppression and filtering processing, thereby improving the accuracy and stability of the output signal frequency of the phase-locked loop circuit.

1. Introduction

According to the principle of the PLL circuit, the accuracy and stability of the input reference signal directly affect the accuracy of the output signal of the PLL circuit.

In the application of MC14552 PLL chip [1], the input reference signal is pre-divided by the built-in R frequency divider as the reference frequency of phase discrimination. The dividing coefficient of R frequency divider can be selected as one of 8, 128, 256, 512, 1024, 2048, 2410, 8192. By using 10MHz signal as input reference source signal, after R frequency divider, the reference frequency of 10 integer multiple phase discrimination can not be obtained, so it is not suitable to select 10MHz signal. After calculation and selection, 10.24 MHz is selected as the input reference signal in this application. The division coefficient of R frequency divider is 1024, and the reference signal of phase discrimination is 10KHz.

There are two ways to generate 10.24MHz signal. One is to attach 10.24MHz crystal to OSC1 and OSC2 pins of MC145152 chip, and generate 10.24MHz signal through its internal oscillating circuit. After R=1024 frequency division, it is used as phase-locked loop reference frequency. But ordinary quartz crystal oscillator can only achieve the frequency stability of E-5. After adopting high-quality quartz crystal and constant temperature control measures, it can achieve the frequency stability of E-11, but it has the shortcomings of frequency drift, high cost or high power consumption. The second method is to connect 10.24MHz signal to OSC1 pin as input signal. After R=1024 pre-dividing, the reference frequency of 10KHz phase-locked loop can also be obtained. When the frequency stability of 10.24 MHz external signal reaches E-11 or above, the output frequency of MC145152 phase-locked loop can reach E-11 or above. Mode 2 is often used in high precision time-frequency domain.

Through the above description, the core technology is to develop a 10.24 MHz reference signal with frequency stability above E-11. It is found that 10.24 MHz signal is not commonly used, usually generated by high stability signal through direct digital synthesis (DDS).

This paper mainly introduces a method to produce 10.24MHz high precision signal by using DDS frequency conversion circuit. As the reference source of MC145152 PLL, the output signal has high stability.

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2. AD9852 chip realizes 10.24MHz frequency conversion

It has been introduced in literature that 10.24 MHz signal can be generated by using 10 MHz signal through DDS device AD9852. However, AD9852 devices have some disadvantages, such as high power consumption, high spurious, unfavorable to circuit miniaturization and so on. According to Nyquist sampling theorem, the maximum output frequency of DDS should be less than FC (input clock)/2, and only 40% FC (input clock) can be achieved in practical application. Therefore, in order to obtain 10.24MHz signal, the 10MHz reference signal must pass at least 3 times of frequency before it can be used as the clock input of AD9852 device (fc >=30MHz). Therefore, it is necessary to design frequency doubling circuit in this scheme. In theory, the multiplier will increase the signal frequency by N times, which will increase the phase noise by 20 log10 (N) dB. Similar N-division will reduce the phase noise by 20 log10 (N) dB. After calculation, the additional phase noise introduced by the 3-fold frequency circuit is 9.5dB, which can not be ignored.

3. AD9832 chip realizes 10.24MHz frequency conversion

After analysis, 10.24MHz signal can be obtained by using 10MHz as reference source signal, which can be directly generated by 10MHz multiplier circuit via DDS device, or by mixing 10MHz signal with 0.24MHz signal. According to Nyquist sampling theorem, 10MHz signal can be used as input clock FC of DDS device. After direct digital frequency synthesis, 0.24MHz signal can be obtained directly.

According to the above idea, only 10 MHz signal can be generated by DDS device to 0.24 MHz signal. Because of the simplified design requirements, it is not suitable to select DDS devices with complex functions such as AD9852/AD9854. Another DDS device, AD9832, has the advantages of low power consumption and simple external circuit. It can accurately preset the output frequency and phase by programming, which can fully meet the design requirements.

3.1. Introduction to the Principle of AD9832 Chip

DDS consists of phase accumulator, accumulator register, waveform memory, D/A converter, and low-pass filter. It uses the sampling theorem to take the phase data as the phase sampling address of the waveform-amplitude memory, completes the phase-to-amplitude conversion by look-up table method, converts the digital waveform amplitude into the analog signal of the required synthesized frequency by D/A converter, and filters the high frequency components of the generated ladder-shaped sine wave with external low-pass filter, and finally outputs the pure positive spectrum. Chord wave signal.

The working principle of AD9832 chip is the same as above, and its output frequency FOUT = MCLK*N/232. In this paper, when MCLK is a 10 MHz reference clock and N is a 0.24 MHz FOUT output, 32-bit control words in AD9832 frequency control word register are written by MCU controller.

By adding 0.24MHz synthesized by AD9832 chip and 10MHz signal mixing, 10.24MHz signal can be obtained. In order to meet the technical requirements of harmonics, phase noise and stability, filter, matching, power amplification and isolation output circuits need to be added. The design principle is shown in Figure 1.

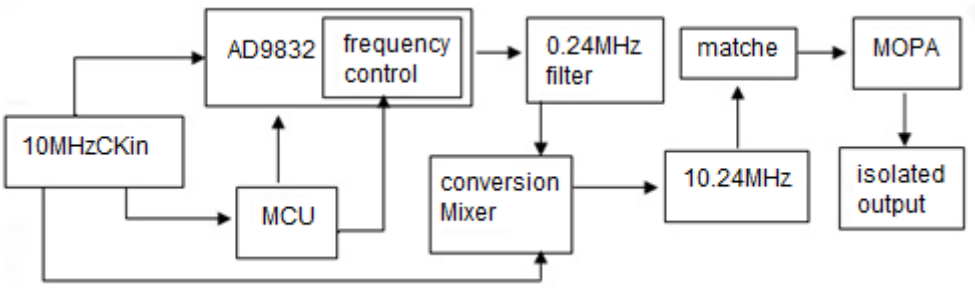

Figure1 Principle of the design

3.2. Introduction of AD9832 Peripheral Hardware Circuit

According to the design principle of Fig. 1, the frequency converter in this paper includes MCU main control unit circuit [4], AD9832 unit circuit, mixing circuit, 3-order elliptical bandpass 0.24MHz filter circuit [5], matching, amplifying and isolating output circuit.

The 0.24MHz output of AD9832 has rich harmonic components and the sinusoidal signal is ladder-like. It must be improved by band-pass filter to filter out the out-of-band stray before it can be used. Elliptic function filter has better performance than other function filters because of its narrow transition band and rapid decline.

The mixing of 0.24MHz signal and 10MHz signal after 3-order elliptic bandpass filtering is obtained by 54HC86 XOR gate (equivalent to adding). The output is square wave. After high Q value, narrowband pass crystal filter circuit and frequency selective amplification, a smooth and pure 10.24MHz sinusoidal wave signal can be obtained.

3.3. AD9832 Device Software Programming

AD9832 communicates according to SPI timing of standard serial interface and according to the timing requirement of AD9832 chip register control word configuration [3], three 16-bit functional registers are assigned successively from SDATA port. Serial data starts from MSB and ends from LSB. Synchronization terminal FCTNC pulls down when operating on functional registers [7]. SCLK connects external 10MHz reference clock signal. Specific register content settings can refer to chip manuals and programming guidelines.

By modifying the frequency control word N and the phase control word P [7], the output frequency and the output phase can be flexibly modified.

3.4. Spectrum Analysis of Output Signal of 2.4 10.24 MHz Signal

The spectrograph is used to observe the 10MHz reference source signal and the final output 10.24MHz spectrum signal as shown in Figure 2. It can be seen that the quality of 10.24 MHz signal and 10 MHz reference source signal is the same after high Q value crystal filter and frequency selective amplification, and the harmonic and clutter components are adequately suppressed.

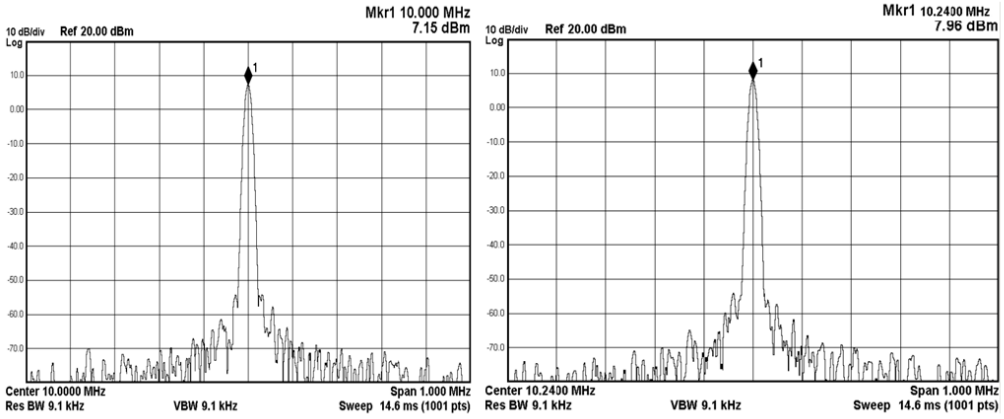

Figure 2 10MHz reference source signal and 10.24MHz output spectrum comparison

Table 1 is a comparison of 10.24 MHz signal technical specifications obtained by the two frequency conversion circuits of AD9832 non-frequency doubling scheme and AD9852 frequency doubling scheme. The comparison includes signal harmonics, power, phase noise and the improvement of the output frequency stability of the phase-locked loop circuit.

It is found that the 10.24 MHz signal can be obtained by mixing 0.24 MHz signal with 10 MHz signal without frequency doubling, and the harmonic and phase noise indexes have reached (far) or better than (near) AD9852 scheme with frequency doubling circuit. At the same time, MC145152 PLL reference source uses frequency converter scheme to generate 10.24 MHz compared with 10.24 MHz ordinary quartz crystal oscillator scheme, and its PLL output frequency stability

improves by three orders of magnitude.

Table 1 Comparison of technical indicators

	10MHzinput signal	**10.24MHz output signal (no multiplier + AD9832 scheme)**	**10.24MHz output signal (3 times frequency circuit + AD9852 solution)**
harmonic	Second: -38.2 dbc Third: -45.3 dbc	second: -53.8dbc third : -70.9 dbc	second: -45.3dbc third : -66.2 dbc
Power	7.15dBm	7.96dBm	7.35dBm
Phase noise	-100.4dbc/1Hz -126 dbc /10Hz -135.1dbc/100Hz -145.4/1kHz -155.2/10kHz -154.3/100kHz	-88.3dbc/1Hz -115.3 dbc /10Hz -130.5dbc/100Hz -138.2/1kHz -145.5/10kHz -146.2/100kHz	-83.5dbc/1Hz -112.3 dbc /10Hz -128.8dbc/100Hz -138.7/1kHz -145.1/10kHz -145.9/10kHz
output signal frequency stability of MC145152 phase-locked loop circuit	MC145152 phase-locked loop circuit reference source uses 10.24MHz frequency converter output signal		
	/	2.6E-11$\sqrt{\tau}$	4.2E-11$\sqrt{\tau}$
	Phase-locked loop reference source uses 0.24MHz ordinary quartz crystal		
	6.1E-8$\sqrt{\tau}$		

4. Conclusion

In this paper, the 10.24 MHz frequency converter is studied and improved. Without using internal or external frequency doubling circuit, the 10 MHz reference source signal is used as the input clock of the digital frequency synthesizer directly, and the frequency conversion of the 10.24 MHz signal is realized. Without frequency doubling circuit, the output signal can be processed more easily in spectrum purity improvement, harmonic and phase noise suppression, and has the advantages of low cost, low power consumption and miniaturization.

References

[1] MC145152 DATASHEET. http://html.alldatasheet.com/html-pdf/77362/MOTOROLA/MC145152/322/1/MC145152.html

[2] Wang Yong, Dong Tianlin. Design of the final frequency conversion stage of Rb atomic frequency standard [B]. Modern Electronic Technology, No.7, 2004, No. 174

[3] AD9832 DATASHEET. http://www.analog.com/static/imported-files/data_sheets/AD9832.pdf

[4] ATmega48 DATASHEET. Http://ishare.iask.sina.com.cn/download/explain.php?fileid=15339134

[5] 74HC86 DATASHEET. Http://focus.ti.com.cn/cn/lit/ds/symlink/sn7486.pdf

[6] Jia Xiaobin, Liu Sixin, Jia Hailiang. Design of elliptic function low-pass filter based on DDS [B]. Electronic design engineering, 2010, 18(9): 171-173

[7] AD9832/ AD9835 Programming Example